FIG 1

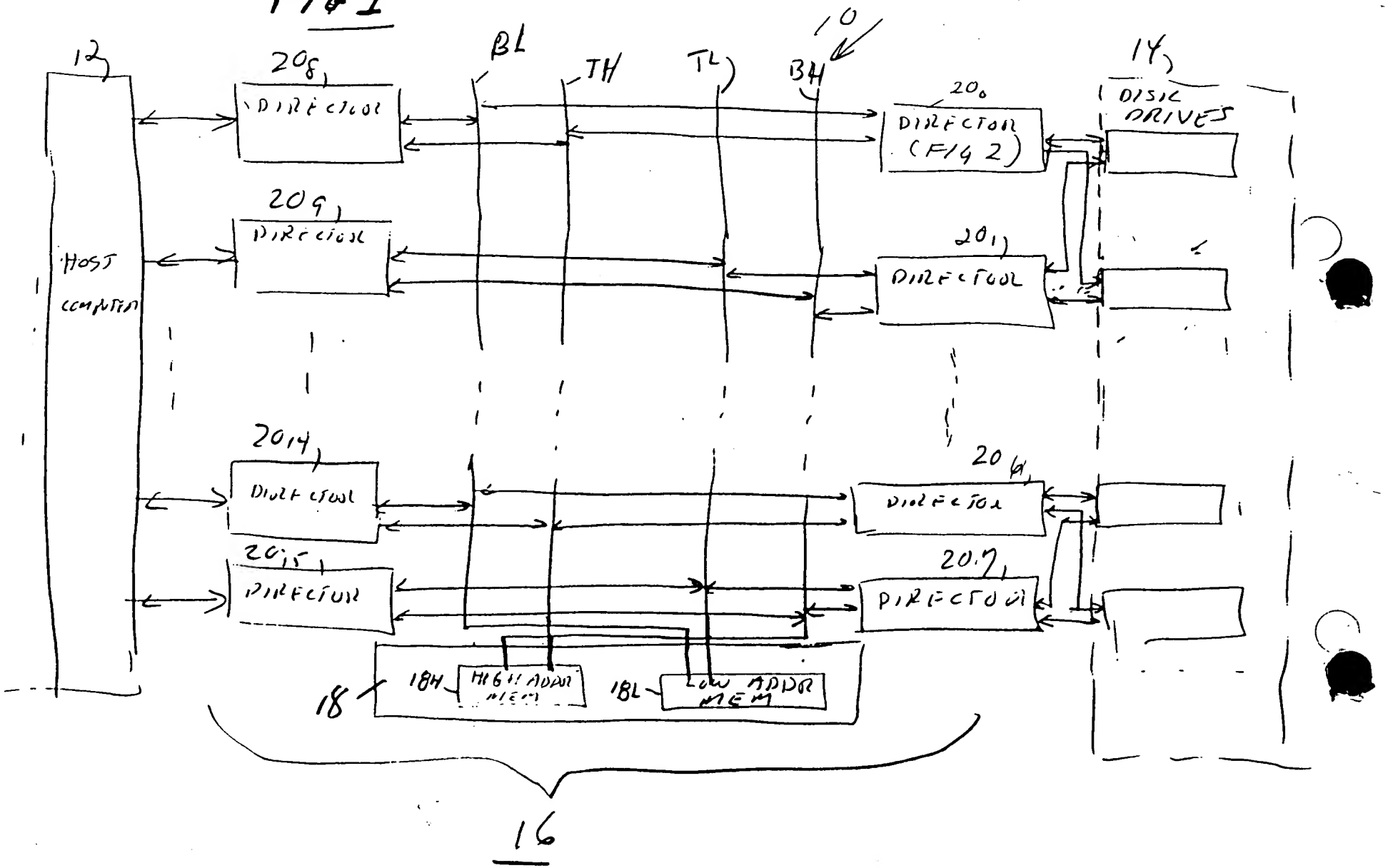
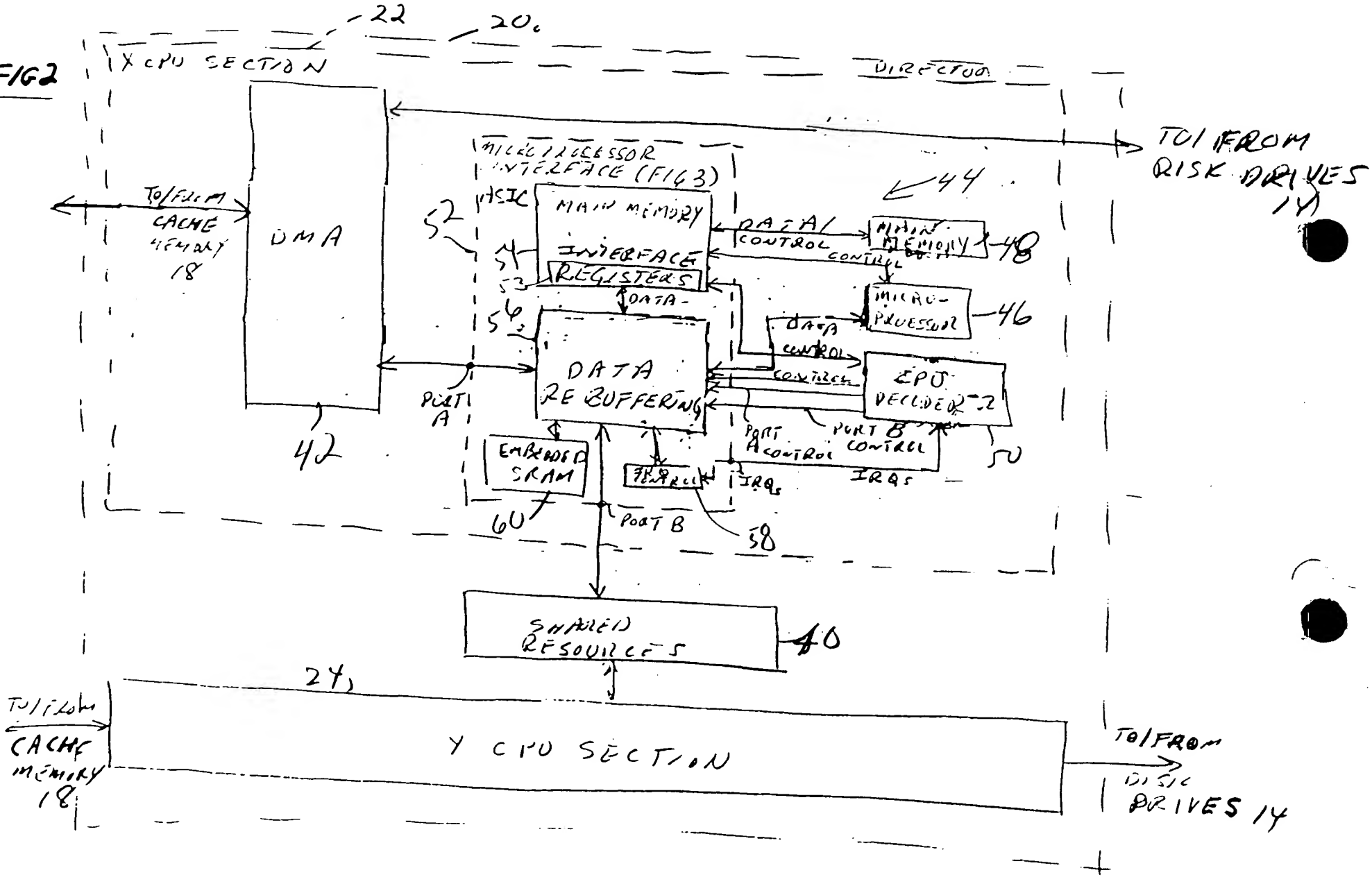


FIG 2



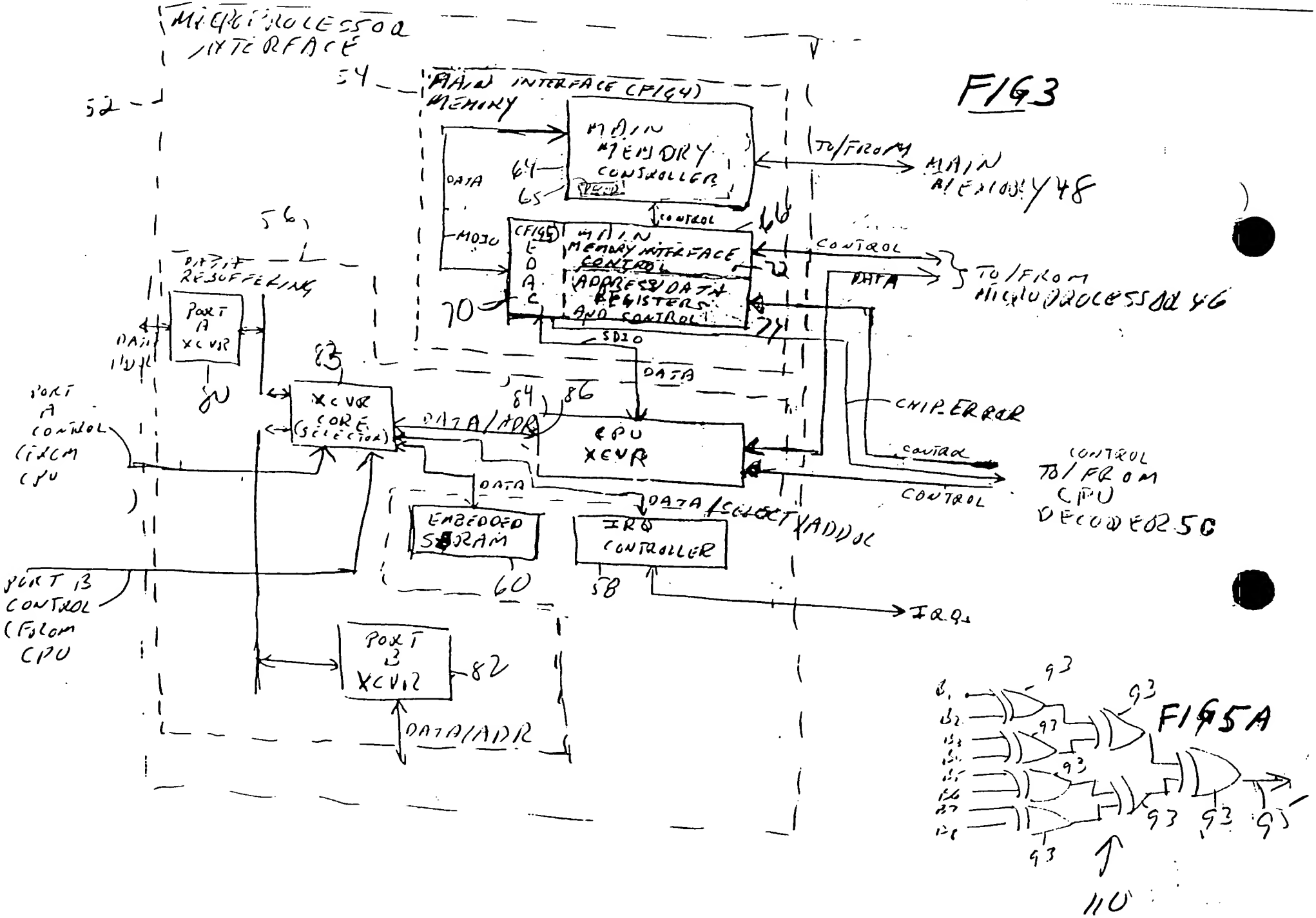

MICROPROCESSOR INTERFACE
52
54
MAIN INTERFACE (FIG 4)
MAIN MEMORY CONTROLLER
DATA
64
65
TEST
TO/FROM MAIN MEMORY 48
CONTROL
66
MODE
(FIG 5)
MAIN MEMORY INTERFACE CONTROL
ADDRESS/DATA REGISTERS AND CONTROL
CONTROL
DATA
TO/FROM MICROPROCESSOR 46
70
72
SDIO
DATA
56
DATA RESOLVING
PORT A XCVR
DATA I/O
83
84
86
XCVR CORE (SELECTION)
PORT A CONTROL (FROM CPU
DATA/ADR
EPU XCVR
CHIP ERROR
CONTROL
CONTROL TO/FROM CPU DECODE 250
DATA
DATA/SELECT/ADDR
EMBEDDED SRAM
IRQ CONTROLLER
60
58
PORT B CONTROL (FROM CPU
IRQ
PORT B XCVR
82
DATA/ADDR

FIG 3

93
110

FIG 5A

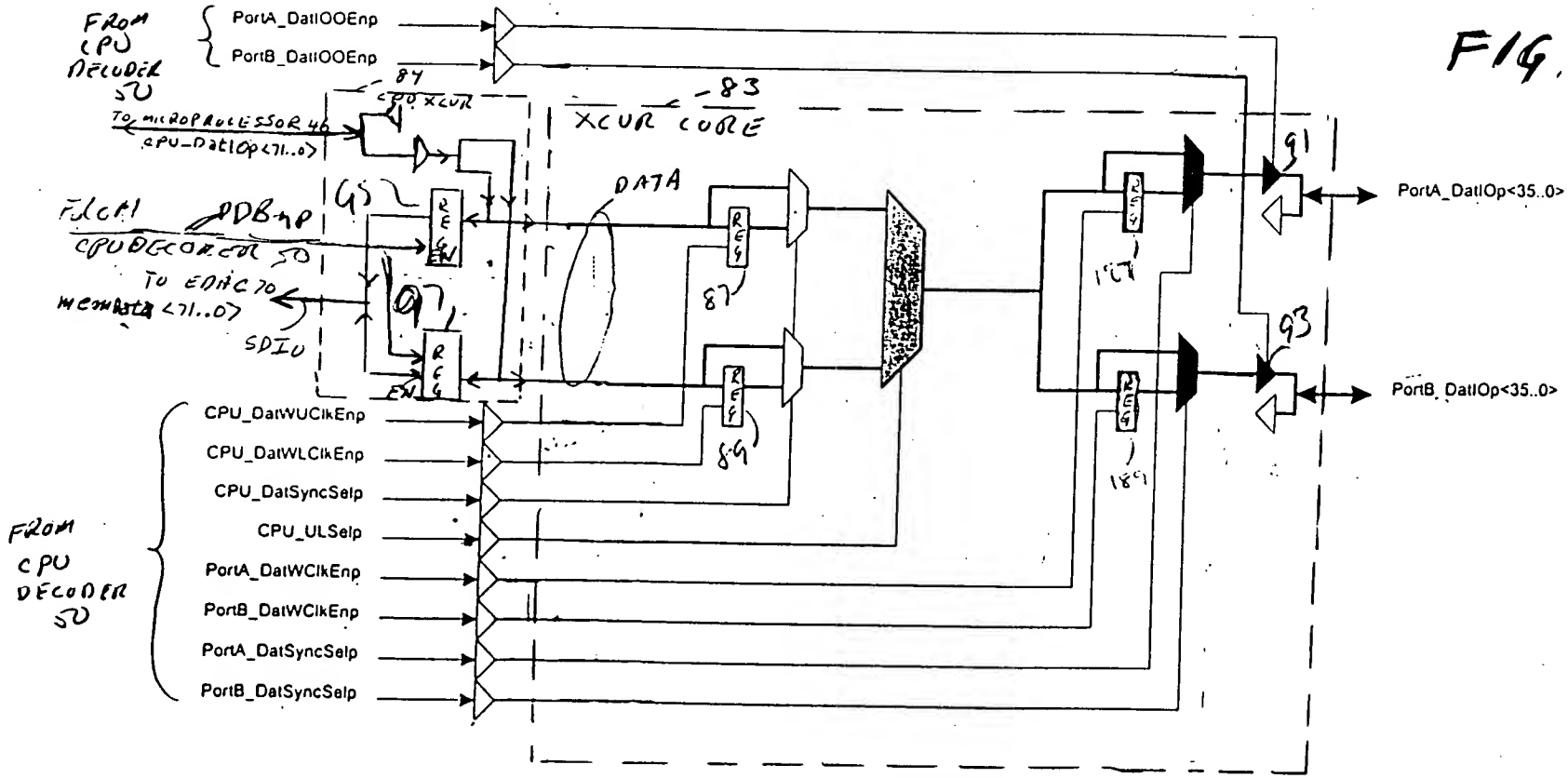

FROM CPU DECODER 50
PortA_DatIOOEnp
PortB_DatIOOEnp
84
CPU XCUR
TO MICROPROCESSOR 46
CPU_DatIOp<71..0>
XCUR
83
CORE
DATA
FROM CPUDECODER 50
TO FDAC 70
MEMDATA <71..0>
SDIU
87
89
91
93
PortA_DatIOp<35..0>
PortB_DatIOp<35..0>
CPU_DatWUClkEnp
CPU_DatWLClkEnp
CPU_DatSyncSelp
CPU_ULSelp
PortA_DatWClkEnp
PortB_DatWClkEnp
PortA_DatSyncSelp
PortB_DatSyncSelp
FROM CPU DECODER 50

FIG. 3A

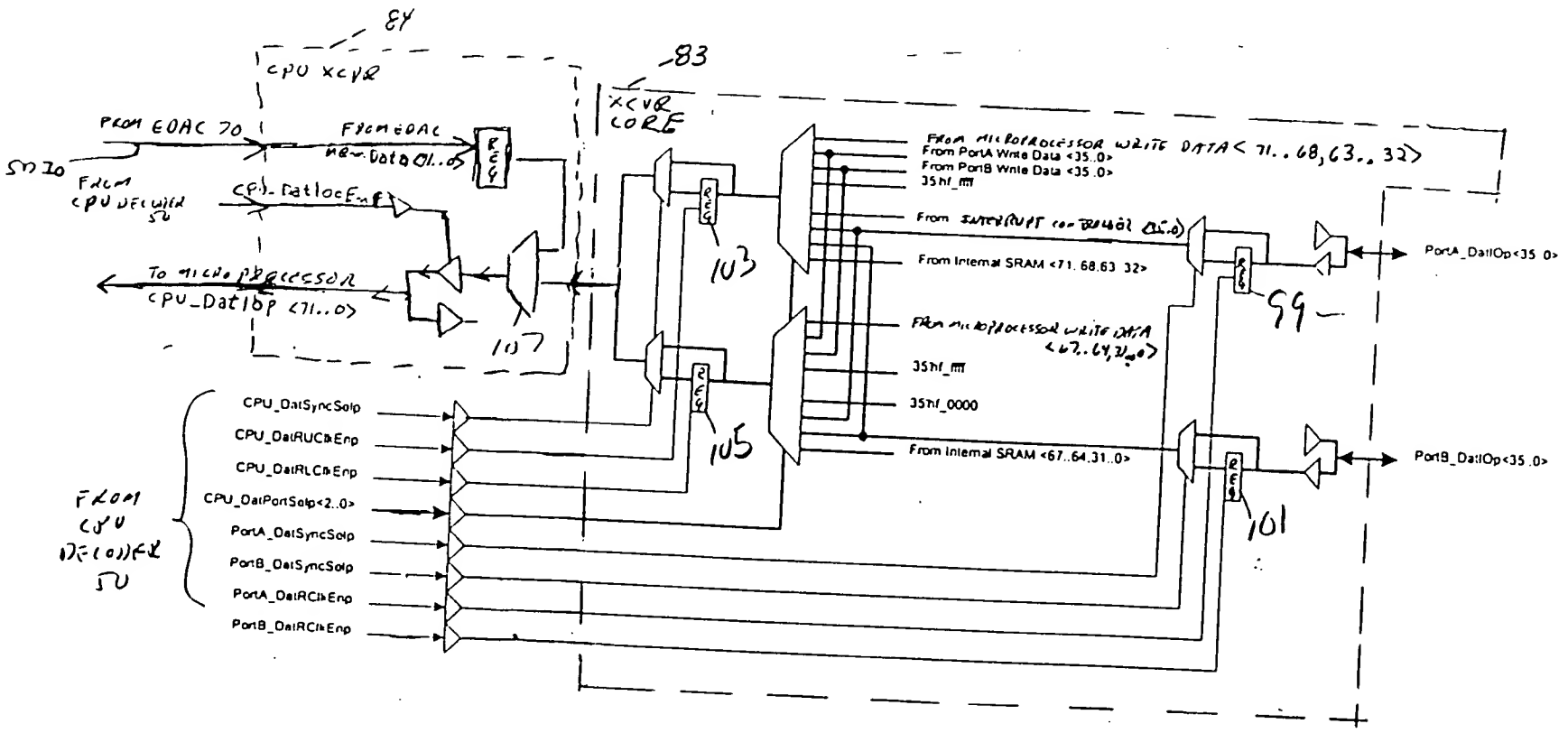
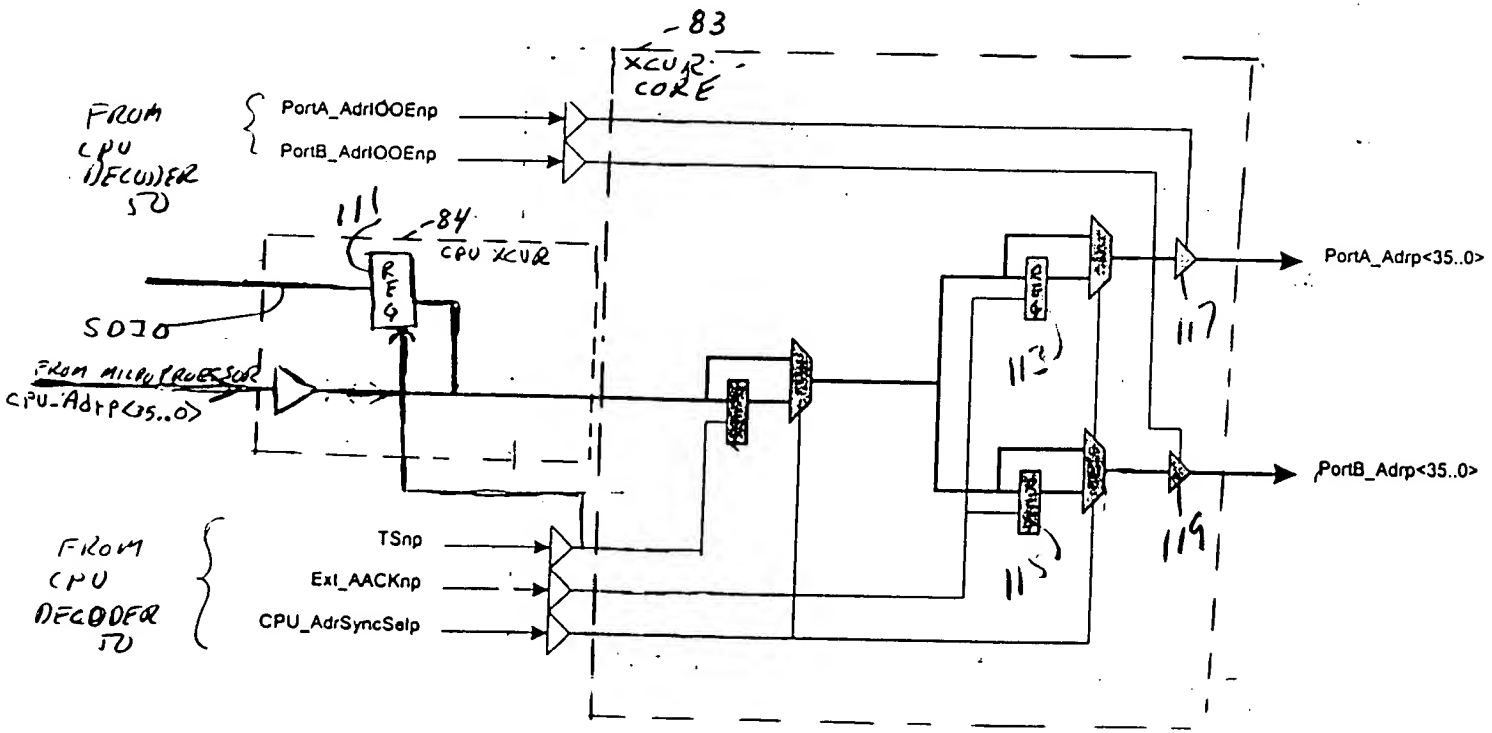

CPU XCVR
XCVR CORE
FROM EOAC TO SM
FROM EOAC
CPU_DatIocEnp
To microprocessor
CPU_DatIOp <71..0>
From microprocessor write data <71..68,63..32>
From PortA Write Data <35..0>
From PortB Write Data <35..0>
35'hf_ffff
From Interrupt controller <35:0>
From Internal SRAM <71..68,63..32>
From microprocessor write data <67..64,31..0>
35'hf_ffff
35'h0_0000
From Internal SRAM <67..64,31..0>
PortA_DatIOp<35..0>
PortB_DatIOp<35..0>
CPU_DatSyncSelp
CPU_DatRUClkEnp
CPU_DatRLClkEnp
CPU_DatPortSelp<2..0>
PortA_DatSyncSelp
PortB_DatSyncSelp
PortA_DatRClkEnp
PortB_DatRClkEnp
FROM CPU
REG
107
103
105
101
99
83
EY

FIG3B

FIG3C


83
XCVR CORE
FROM CPU DECODER 52
PortA_Adrl0OEnp
PortB_Adrl0OEnp
111
84
CPU XCVR
REG
SOJO
FROM MILBUS PROCESSOR
CPU-Adrp<35..0>
FROM CPU DECODER 52
TSnp
Ext_AACKnp
CPU_AdrSyncSelp
PortA_Adrp<35..0>
PortB_Adrp<35..0>
117
119

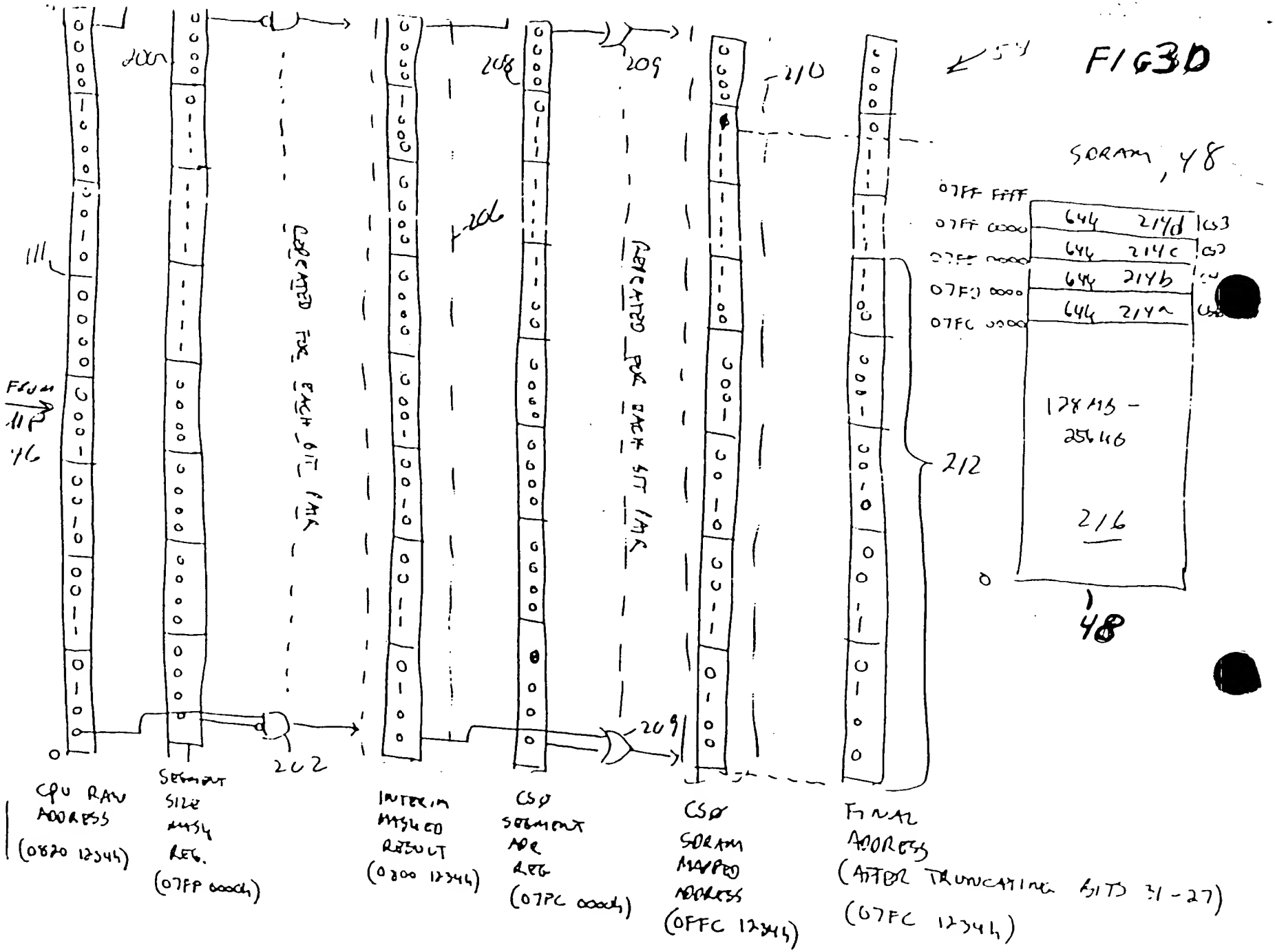
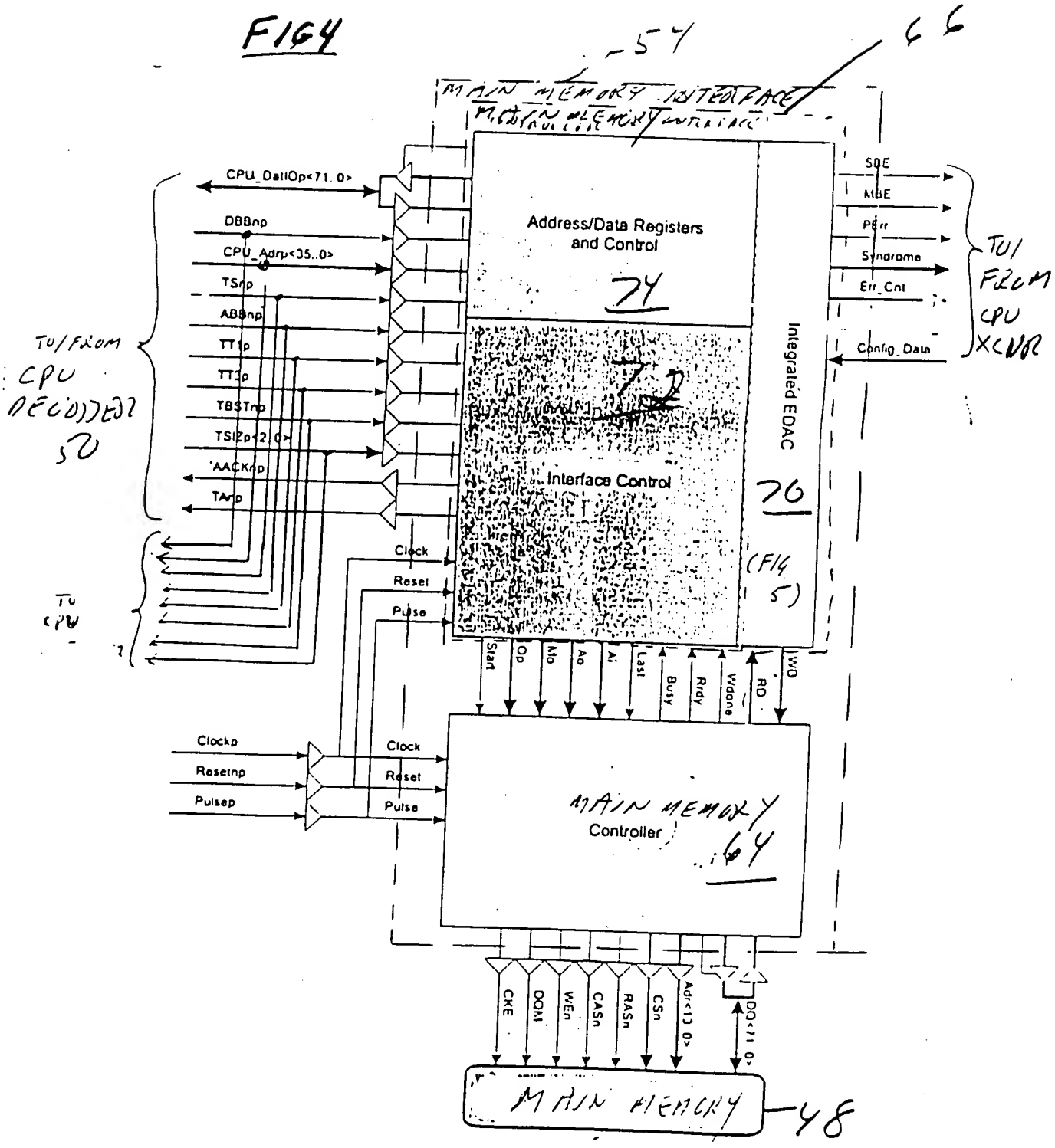
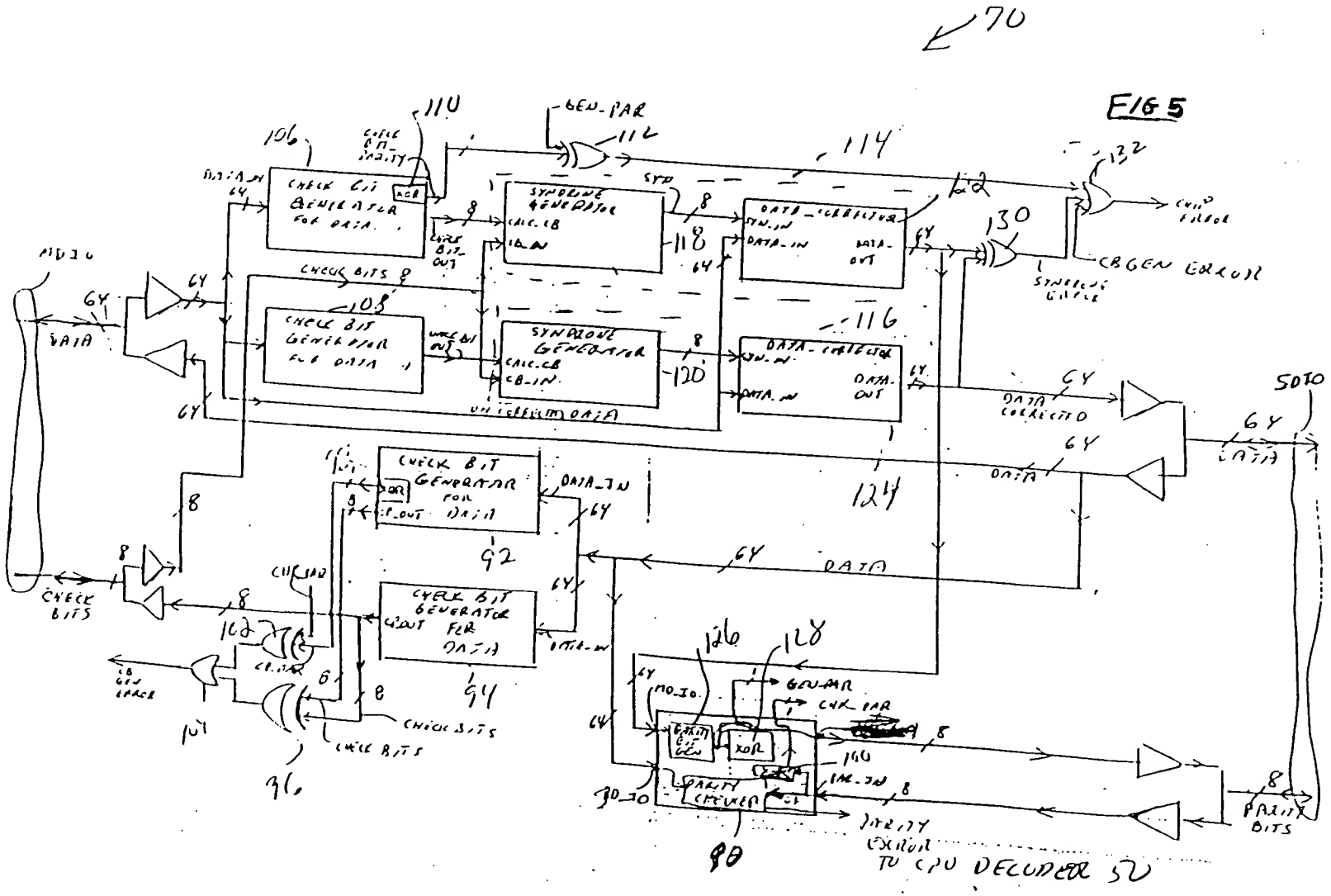
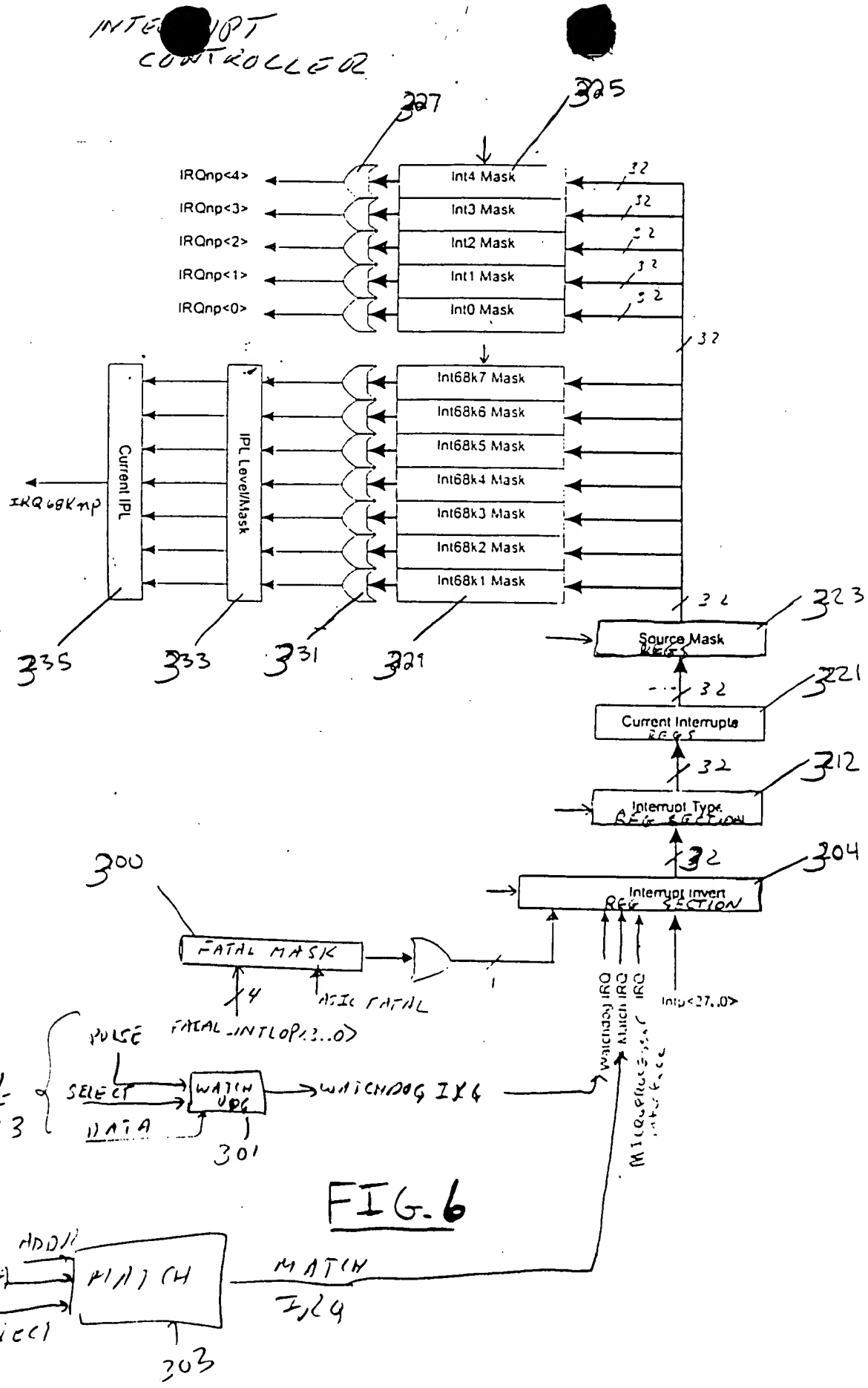


FIG3D
SRAM, 48
07FF FFFF
07FF 0000
07FE 0000
07FD 0000
07FC 0000
64K 214d CS3
64K 214c CS2
64K 214b CS1
64K 214a CS0
128K15 - 25646
216
0
48
212
210
209
208
206
202
111
FROM IIP 46
CPU RAW ADDRESS (0820 12344)
SEGMENT SIZE MASK REG. (07FF 0000h)
CONCATENATED FOR EACH BIT MASK
INTERIM MASKED RESULT (0800 12344)
CS0 SEGMENT ADR REG (07FC 0000h)
CONCATENATED FOR EACH BIT MASK
CS0 SRAM MAPPED ADDRESS (0FFC 12344)
FINAL ADDRESS (AFTER TRUNCATING BITS 31-27) (07FC 12344)

FIG 4


MAIN MEMORY INTERFACE
MAIN MEMORY CONTROLLER
Address/Data Registers and Control
74
Interface Control
72
Integrated EDAC
76
(FIG 5)
CPU_DatIOp<71..0>
DBBnp
CPU_Adrp<35..0>
TSnp
ABBnp
TT1p
TT3p
TBSTnp
TSIZp<2..0>
AACKnp
TAnp
TO/FROM CPU DECODED 50
TO CPU
Clock
Reset
Pulse
Start
Op
Mo
Ao
Ai
Last
Busy
Rrdy
Wdone
RD
WD
Clockp
Resetnp
Pulsep
MAIN MEMORY Controller
64
CKE
DQM
WEn
CASn
RASn
CSn
Adr<13..0>
DQ<71..0>
MAIN MEMORY
48
SDE
MDE
PErr
Syndrome
Err_Cnt
Config_Data
TO/FROM CPU XCVR




INTERRUPT CONTROLLER
327
325
IRQnp<4>
IRQnp<3>
IRQnp<2>
IRQnp<1>
IRQnp<0>
Int4 Mask
Int3 Mask
Int2 Mask
Int1 Mask
Int0 Mask
32
Int68k7 Mask
Int68k6 Mask
Int68k5 Mask
Int68k4 Mask
Int68k3 Mask
Int68k2 Mask
Int68k1 Mask
Current IPL
IPL Level/Mask
IRQ68Knp
335
333
331
329
Source Mask
323
Current Interrupts
321
Interrupt Type
312
Interrupt Invert
304
300
FATAL MASK
FATAL_INTLOP<3..0>
NMI FATAL
Intp<27..0>
Watchdog IRQ
Match IRQ
PULSE
SELECT
DATA
WATCHDOG
WATCHDOG IX4
301
FIG. 6
MATCH
303
IX4

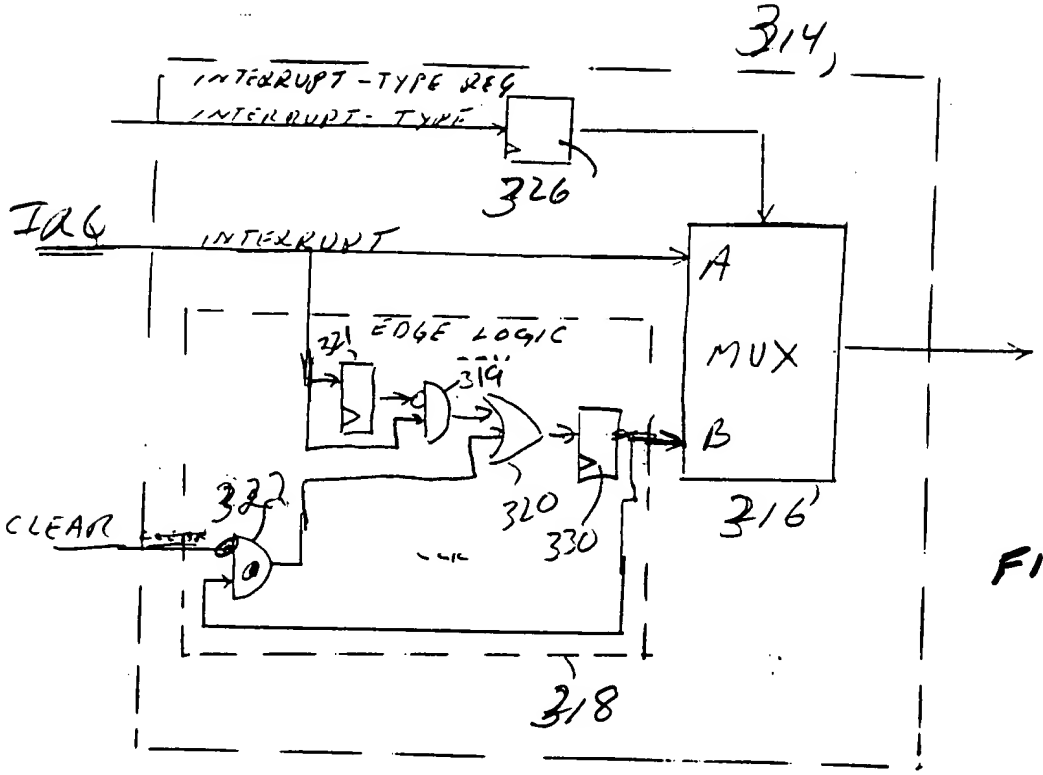


FIG 8

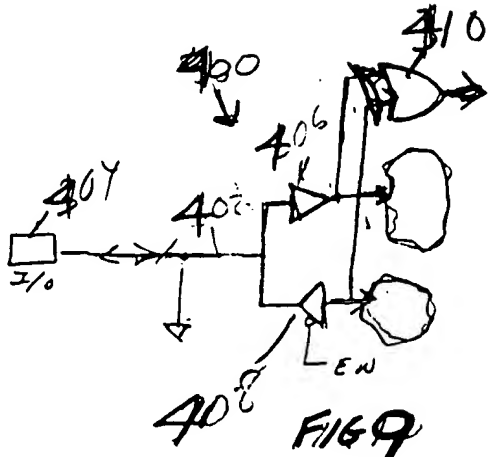


FIG 9

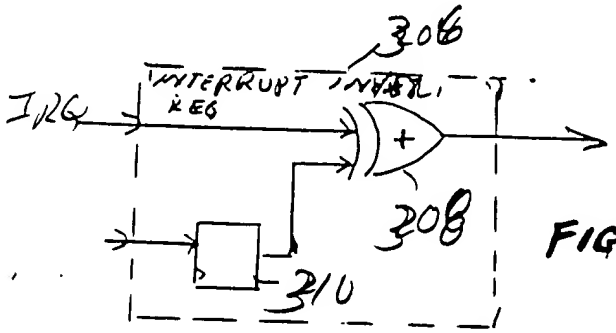


FIG 7